REMARKS

Claims 1-8 are pending with claims 5-7 having been withdrawn from consideration. By this amendment, the drawings and specification are amended, claim 2 canceled and claim 1 amended. Reconsideration in view of the above amendments and the following remarks is respectfully requested.

The Office Action objects to the specification for a number of informalities. Applicant has generally amended the specification in accordance with the Examiner's recommendations. However, Applicant respectfully submits that in relation to the dc blocking first capacitor element 54 and dc blocking third capacitor element 58 that this terminology is correct and that first and third, respectively, modify the capacitor element not the blocking. Additionally, Applicant respectfully submits that like reference numbers are used to describe like components throughout the specification. Accordingly, the corresponding description of elements 13 and 22 of Fig. 3(a) can at least be found on pages 11 and 12 of the specification, elements 32 and 33 of 5(c) on page 18 of the specification, element 211 of Figs. 10(c), 11(b), and 11(d) on page 28 of the specification. In relation to Fig. 11(a) Applicants have amended the specification to include a description of Fig. 11(a).

In relation to elements 307, 308, 313, 314, 315 of Figs. 15 and 16 Applicant submits the attached amendment supplies a corresponding description of these elements as requested by the Examiner.

Additionally, Applicant has amended the terms DUROID and TEFLON as recommended by the Examiner.

Accordingly, withdrawal of the rejection to the specification if respectfully requested.

Regarding the drawings, Applicant submits herewith a request for approval of drawing corrections. In particular, Applicant has amended the drawings in accordance with the Examiner's recommendations. However, in relation to Figs. 1, 2B, 2C, 3A, 3B, 4, 5B, 6A, 6B, 9, 10A-10D, 11A-11D, 12A-12D, 13A-13C and 14A-

14C, Applicant respectfully submits that MPEP 608.02 does not specify a specific cross-hatching for dielectrics. Accordingly, Applicant respectfully request the Examiner to clarify the objection to the drawings or to withdraw the outstanding objection. Withdrawal of the objection to the drawings is respectfully requested.

The Office Action rejects claim 1 under 35 U.S.C. §102(b) as anticipated by either Japanese Application No. 62-316319 to Shigaki (hereinafter "Shigaki") or U.S. Patent No. 5,493,263 to Tozawa (hereinafter "Tozawa"). This rejection is respectfully traversed.

Claim 1 recites, *inter alia*, a microstrip line comprising a ground conductor layer, a dielectric layer disposed on the ground conductor layer, a linear conductor layer disposed on the dielectric layer to have a linear configuration, the linear conductor layer having a wider portion in an upper part of a cross section thereof taken in a direction perpendicular to a direction in which the linear conductor layer extends and a narrower portion in a lower part of the cross section, the narrower portion being smaller in width than the wider portion and a substrate for holding the ground conductor layer, the substrate being located under the ground conductor layer composed of a dielectric material, wherein the dielectric layer has a dielectric constant higher than a dielectric constant of the substrate.

Therefore, for example, even if the dielectric constant of the dielectric layer composing the microstrip line of the present invention is set higher than the dielectric constant of the substrate holding the ground conductor layer, the linear conductor layer is composed of the wider and the narrower portions and having a T-shaped cross section, such that a high impedance can be achieved in the line.

In contrast, Tozawa discloses, as illustrated in Fig. 1, a microstrip line composed of a dielectric substrate 10, a conducting strip 14 and a upper conductor 16, which has a T-shaped cross section, formed on the dielectric substrate 10, and a grounded conductor formed on the back surface of the dielectric substrate 10.

However, Tozawa at least fails to teach, suggest or disclose a substrate for

holding the ground conducting layer from the back surface. Moreover, Tozawa discloses that the conducting strip 14 has a width lager than that of the base 16a of the upper conductor 16 as provided between the dielectric substrate 10 and the upper conductor 16, which is different from the amended claim 1 were the narrower portion of the linear conductor layer is directly in contact with the dielectric layer. Hence, the linear conductor in Tozawa does not substantially have a T-shape.

Further in contrast, Shigaki discloses, as illustrated in Fig. 1, a microstrip line composed of a dielectric substrate 1, a conductor 2 having a T-shape cross section and formed on the dielectric substrate 1, and a ground conductor 3 formed on the back surface of the dielectric substrate 1. However, Shigaki at least fails to teach, suggest or disclose a substrate for holding the ground conductor layer from the back surface as claimed.

Accordingly, since the cited references fail to teach, suggest or disclose each and every feature as claim of claim 1, the reference fail to render obvious claim 1. Withdrawal of the rejection of claim 1 under 35 U.S.C. §102(b) is respectfully requested.

The Office Action rejects claims 1, 2, 3, and 4 under 35 U.S.C. §103(a) as unpatentable over Japanese Patent Application No. 5-37207 to Nakajima (hereinafter "Nakajima"). This rejection is respectfully traversed.

Nakajima disclose, as illustrated in Fig. 1, a microstrip line composed of a metal film 4, an insulating film 2 and a metal thin film line 3 sequentially formed on a substrate 1. However, Nakajima at least fails to disclose that the metal thin film line 3 has a T-shape cross section structure, and the high-low relation between the dielectric constant of the insulating film 2 and that of the substrate 1. Accordingly, since Nakajima fails to teach or suggest the high-low relation between the dielectric constant of the dielectric layer and that of the substrate, Applicant respectfully submits that the cited reference, fails to teach, suggest or disclose each and every feature of the claims.

Accordingly, the cited references fail to render obvious claims 1, 2, 3 and 4. Withdrawal of the rejection of these claims under 35 U.S.C. §103(a) is respectfully requested.

Applicant respectfully submits the application is in condition for allowance. Favorable reconsideration and prompt allowance are respectfully requested.

Should the Examiner believe anything further is desirable in order to place the application in even better condition for allowance. The Examiner is encouraged to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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Marked-Up Version of Amendments

IN THE SPECIFICATION:

Please amend the Specification as follow:

Page 1, paragraph 3:

FIG. 15 shows a conventional RF circuit. FIG. 16 shows a plan configuration of an RF semiconductor device in which the RF circuit shown in Fig. 15 is implemented in a substrate. In FIG. 16, the same components as shown in FIG. 15 are designated by the same reference numerals. Specifically, the RF circuit comprises a DC blocking capacitance 307, a register 308, a drain terminal 313, a gate terminal 314 and a source terminal 315.

Page 7, paragraph 3:

FIGS. 2A [to] , 2B and 2C are structural cross-sectional views illustrating the individual process steps of a method for fabricating the microstrip line according to the first embodiment;

Page 7, paragraph 6:

FIGS. 5A [to] , 5B and 5C are structural cross-sectional views illustrating the individual process steps of a method for fabricating the microstrip line according to the second embodiment;

Page 8, paragraph 5:

FIGS. 10A [to] , 10B, 10C, and 10D are structural cross-sectional views illustrating the individual process steps of a method for fabricating the microstrip line according to the third embodiment;

Page 8, paragraph 6:

FIGS. 11A [to] , 11B, 11C and 11D are structural cross-sectional views illustrating the individual process steps of a method for fabricating the microstrip line

according to the third embodiment;

Page 8, paragraph 7:

FIGS. 12A [to] <u>, 12B, 12C and</u> 12D are structural cross-sectional views illustrating the individual process steps of a method for fabricating the microstrip line according to the third embodiment;

Page 8, paragraph 8:

FIGS. 13A [to] <u>, 13B and</u> 13C are structural cross-sectional views illustrating the individual process steps of a method for fabricating the microstrip line according to the third embodiment;

Page 9, paragraph 1:

FIGS. 14A [to] <u>, 14B and</u> 14C are structural cross-sectional views illustrating the individual process steps of a method for fabricating the microstrip line according to the third embodiment;

Page 12, paragraph 2 continuing onto page 13:

Next, as shown in FIG. 3B, the third resist film 23 <u>shown in Fig. 3A</u> is removed and an unwanted portion of the Au layer in the upper part of the multilayer structure composing the second-layer forming layer 16A shown in Fig. 3A is removed by using an etchant composed of potassium iodine (KI). Subsequently, an unwanted portion of the Ti layer in the lower part of the multilayer structure composing the second-layer forming layer 16A is removed by using hydrogen fluoride (HF), whereby the second-layer forming layer 16A is patterned into the second layer 16 of the linear conductor layer 14. Thereafter, the second resist film 22 shown in Fig. 3A is removed by using a resist remover and then the protective insulating film 18 composed of a silicon dioxide is deposited entirely over the dielectric layer 13 so as to cover the linear conductor layer 14.

Page 14, Paragraph 3 continuing onto page 15:

Although the protective insulating film 18 composed of the silicon dioxide has been filled in the space between the wider portion 14b of the linear conductor layer 14 and the dielectric layer 13 in order to protect the strip line, it is preferred not to fill the protective insulating film 18 in terms of operation characteristics. In the case of filling the protective insulating film 18, therefore, a low dielectric film having a relatively low dielectric constant such as an organic material composed of, e.g., benzocyclobutene, [duroid] <u>DUROID</u> , or a polymide film is use preferably.

Page 18, paragraph 1:

Referring to [the drawings] <u>figures 5A-5C, 6A and 6B,</u> a description will be given to a method for fabricating the microstrip line thus constituted.

Page 19, paragraph 1:

Next, as shown in FIG. 5C, the narrower-portion formation region of the dielectric layer 33 is exposed by lifting off the first resist film 41 <u>shown in Fig. 5B</u>. Then, the first layer 35 of the linear conductor layer composed of WSiN is deposited by RF sputtering. Thereafter, a second resist film 42 is coated on the deposited first layer 35 and formed into a line pattern with a width of about 5 μm by lithography so as to include the narrower-portion formation region. Subsequently, the first layer 35 is etched back by using the formed second resist film 42 as a mask and using CF_4 to be formed into a pattern including the narrower portion 34a. Thereafter, sintering is performed in an oxygen ambient at a temperature of about 450 °C to recrystallize the dielectric layer 33 and thereby increase the dielectric constant of the dielectric layer 33.

Page 20, paragraph 1:

Next, as shown in FIG. 6B, the third resist film 43 <u>shown in Fig. 6A</u> is removed and an unwanted portion of the Au layer in the upper part of the multilayer structure of the second-layer forming layer [36a] <u>36A</u> is removed by using an etchant composed of KI. Subsequently, an unwanted portion of the Ti layer in the lower part

of the multilayer structure of the second-layer forming layer 36A shown in Fig. 6A is removed by using hydrogen fluoride, whereby the second-layer forming layer 36A is patterned into the second layer 36 of the linear conductor layer 34.

Page 23, paragraph 4 continuing onto page 24:

Although the second embodiment has used GaAs in the substrate 31, an inorganic material composed of a glass material such as Si or quartz or of alumina or an organic material composed of polystyrene or [Teflon] TEFLON may also be used instead.

Page 24, paragraph 4:

A third embodiment of the present invention will be described with reference to [the drawings] Figures 7-14C inclusive.

Page 28, paragraph 2:

FIGS. 10A [to 14C] to 10D, 11A to 11D, 12A to 12D, 13A to 13C and 14A to 14C show the cross-sectional structures of the RF semiconductor device according to the third embodiment in the individual process steps. For the sake of simplicity, the description will be given to a method for forming, over the substrate 211, a region different from the region 50 shown in FIG. 7 and including a FET formation region 1 in which a FET as an amplifying element is to be formed and a line formation region 2 in which a microstrip line is to be formed, as shown in FIG. 10A.

Page 29, paragraph 1:

Next, mesa etching is performed with respect to the FET formation region 1. Subsequently, a first resist film 251 is coated on the substrate 211 and formed into a line pattern [252a] 251a with a width of about 0.2 μm, which is for determining the gate length of the FET, in the FET formation region 1 by lithography using a phase shifting method. Thereafter, a first protective insulating film 212 composed of SiO_2 with a thickness of about 0.2 μm is deposited over the entire surface of the substrate 211 by ion beam sputtering using the first resist film 251 as a mask.

Page 29, paragraph 2:

Next, as shown in FIG. 10B, the first resist film 251 shown in Fig. 10A is lifted off and then a second protective insulating film 213 composed of SiN with a thickness of about 0.3 μm is formed by CVD entirely over the substrate 211 including the first protective insulating film 212.

Page 29, paragraph 4 continuing onto page 30:

Next, as shown in FIG. 10D, a second resist film 252 covering the FET formation region 1 shown in Fig. 10A is formed. Then, a layer 215B forming the second layer of the ground electrode and composed of Au with a thickness of about 2.5 μm is formed by plating. Subsequently, a layer 215C forming the third layer of the ground electrode and composed of a multilayer structure of Pt with a thickness of about 0.2 μm and Ti with a thickness of about 0.02 μm is formed by vapor deposition again.

Page 30, paragraph 1:

Next, as shown in FIG. 11A, the second resist mask 252 is removed and the layer 215A forming the first layer in the FET formation region 1 is removed therefrom by using a KI etchant and hydrogen fluoride, whereby a ground electrode 215 composed of the first-layer forming layer 215A, the second-layer forming layer 215B, and the third-layer forming layer 215C is formed in the line formation region 2. Subsequently, a third protective insulating film 216 composed of SiN with a thickness of about 0.3 μ m is deposited over the entire surface of the substrate 211.

Page 30, paragraph 2:

Next, as shown in FIG. 11B, a third resist mask 253 having an opening pattern in the line formation region 2 is formed on the third protective insulating film 216 by lithography. Subsequently, [RIE] Reactive Ion Etching (RIE) etching is performed with respect to the third protective insulating film 216 by using the third resist film

253 as a mask, thereby exposing the ground electrode 215.

Page 30, paragraph 3 continuing onto page 31:

Next, as shown in FIG. 11c, the third resist film 253 shown in Fig. 11A is removed and then a dielectric layer 217 composed of STO with a thickness of about 0.5 μm is deposited entirely over the substrate 211 including the line formation region 2 by RF sputtering for which the substrate temperature is adjusted to about 300 °C.

Page 31, paragraph 1:

Next, as shown in FIG. 11D, the portion of the dielectric layer 217 included in the FET formation region 1 shown in Fig. 11A is removed by a milling method using a fourth resist mask 254 covering the line formation region 2 of the dielectric layer 217.

Page 31, paragraph 2:

Next, as shown in FIG. 12A, the fourth resist mask 254 shown in Fig. 11D is removed and then a layer 218A forming the first layer of the linear conductor layer and composed of WSiN with a thickness of about 0.1 μm is deposited over the entire surface of the substrate 211 by RF sputtering. Thereafter, the dielectric layer 217 is recrystallized by performing sintering in an oxygen ambient at a temperature of about 450 °C.

Page 32, paragraph 2:

Next, as shown in FIG. 12D, the sixth resist film 256 shown in Fig. 12C is removed and then a seventh resist film 257 having opening patterns for exposing the source/drain formation regions of the FET formation region 1 is formed on the substrate 211 by lithography. Subsequently, etching is performed with respect to the first protective insulating film 212 by using hydrogen fluoride and using the formed seventh resist film 257 as a mask, thereby exposing the source/drain formation regions of the top surface of the substrate 211.

Page 36, paragraph 2:

Although the space between the wider portion 225b of the linear conductor layer 225 and the dielectric layer 217 is filled with the fourth protective insulating film 222 composed of SiN in the present embodiment, the space may be filled preferably with a material having a lower dielectric constant such as an inorganic thin film composed of, e.g., SiO_2 or with an organic thin film composed of BCB, [Duroid] DUROID, or the like.

IN THE CLAIMS:

1. (Amended) A microstrip line comprising:

a ground conductor layer;

a dielectric layer [formed] disposed on the ground conductor layer; [and]

a linear conductor layer [formed] disposed on the dielectric layer to have a linear configuration, the linear conductor layer having a wider portion in an upper part of a cross section thereof taken in a direction perpendicular to a direction in which the linear conductor layer extends and a narrower portion in a lower part of the cross section, the narrower portion being smaller in width than the wider portion and a substrate for holding the ground conductor layer, the substrate being located under the ground conductor layer composed of a dielectric material, wherein the dielectric layer has a dielectric constant higher than a dielectric constant of the substrate.